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EXAMINER	
DINH, NGOC V	
ART UNIT	**PAPER NUMBER**
2187	7

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/963,334	PEREIRA, JOSE P.	
	Examiner	Art Unit	
	NGOC V DINH	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-69* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-69* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2,4,5,6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A. A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-4, 8-11, 13, 58-69 are rejected under 35 U.S.C.102 (e) as being anticipated by Betchtolsheim et al. [6,377,577].

1.As per claims 1-4, 8-11, 13:

Betchtolsheim teaches a content addressable memory (CAM) device [210, fig. 2] comprising:

a first plurality of storage circuits to store an upper value [e.g., upper bound]; a second plurality of storage circuits to store a lower value [e.g., lower bound]; and a plurality of compare circuits to determine if a first comparand value is within a range of values defined by the upper value and the lower value.

Betchtolsheim further teaches the CAM device, wherein the first comparand value is a field of bits within a second comparand value; each of the first plurality of storage circuits includes a memory element to store at least one bit of the upper value; each of the plurality of compare circuits includes circuitry to compare a bit of the first comparand to a bit of the upper value and to output a result signal in a first state if the bit of the first comparand is greater than the bit of the upper value and to output the result signal in a second state if the bit of the first comparand is less than the bit of the upper value [abstract; col. 2, lines 51-65; col. 4, line34-47; col. 5, line 57 to col. 6, line 9]. Inherently, Betchtolsheim teaches The CAM device wherein the upper and lower value comprise a plurality of bits ordered from a most significant bit to a least significant bit, and wherein each of the plurality of compare circuits is adapted to store a respective one of the plurality of bits and to compare the one of the plurality of bits to a respective bit within the first comparand value. This is because in the buffer or register of a computer system, the addressable structure that comprises two fields

constituting respectively of the most significant bits and least significant bits emanating from the combination. In data communication, the most significant bits are closer to the beginning of the data frame than the least significant bits. This has an advantage of allowing processing of data [e.g., comparison process] to be processed with only same of the most significant bits available at the beginning of data frame, thus increasing comparison process.

2. As per claims 58-64:

The claimed elements in the memory device in claims 1-14 are no more than means for carrying out the corresponding steps in the method of claims 58-64. Therefore, claims 58-64 are rejected for the same reason as set forth in claims 1-14.

3. As per claims 65-69:

Claims 65-69 is written in means plus same function format as claims 1-14 and 58-60, therefore the same rejection is applied.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 15, 18, 20-22, 29-32, 45, 48-54 are rejected under 35 U.S.C.102 (b) as being anticipated by Moughanni et al. [6,049,876].

4. As per claims 15, 18, 20-22, 29, 45:

Moughanni teaches a system comprising: a processor and a content addressable memory (CAM) [fig. 1; 50, 52, fig. 6]; a first storage circuit to store a first boundary value [e.g., upper bound]; and a first compare circuit to compare a comparand value to the first boundary value, the first compare circuit including circuitry to output a first result signal in a first state if the comparand value is greater than the first boundary value and in a second state if the comparand value is less than the first boundary value;

a second storage circuit to store a second boundary value [e.g., lower bound] and a second compare circuit to compare a comparand value to the second boundary value,

the second compare circuit including circuitry to output a second result signal in the first state if the comparand value is less than the second boundary value and in the second state if the comparand value is greater the second boundary value [col. 3, line 57 to col. 4, line 60].

Moughanni further teaches a first compare circuit coupled to receive the first value from the first storage circuit and having a select input to receive a level select signal [52, fig. 6], the first compare circuit being adapted to compare a comparand value to the first value and to assert a beyond boundary signal if the level select signal is in a first state and if the comparand value is greater than the first value, the first compare circuit being further adapted to assert the beyond-boundary signal if the level select signal is in a second state and if the comparand value is less than the first value [col. 3, line 55 to col. 4, line 60].

5. As per claims 30-32:

Moughanni further teaches a first input to receive a first signal representative of the comparand value; a second input to receive a second signal representative of a complement of the comparand value; and a select circuit coupled to the first input and the second input to select, according to a state of the level select signal, either the first signal or the second signal to be output to the compare circuit for comparison with the first value; the first value is representative of an upper boundary value when the level select signal is in the first state, and wherein the first value is representative of a lower boundary value when the level select signal is in the second state [col. 3, line 55 to col. 4, line 60].

Inherently, Moughanni teaches the select circuit is a multiplexer having a control input coupled to receive the level select signal and having first and second ports coupled respectively to the first and second inputs.

6. As per claims 48-54:

Moughanni teaches the CAM device further includes a second plurality of CAM cells to store a data value, the second plurality of CAM cells being adapted to compare the data value with a second comparand value in a compare operation and to output a first result signal indicative of whether the second comparand value is equal to the data

value; the first plurality of CAM cells and the second plurality of CAM cells are each included within a first row of CAM cells within the CAM device; the first comparand value and the second comparand value each constitute a respective field of bits within a third comparand value; the CAM device is further responsive to the first instruction from the processor to store a second boundary value in the first plurality of CAM cells, and the first plurality of CAM cells being further adapted to compare the second boundary value with the second comparand in the compare operation and to output a second result-signal indicative o f whether the first comparand value is less than the second boundary value; the CAM device includes multiple independently searchable storage blocks each including a plurality of CAM cells therein, the first plurality of claim cells being included within the plurality of CAM cells in one of the searchable storage blocks; the CAM device further includes a block configuration [fig. 3-5; col. 3, line 44 to col. 4, line 60].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-7 are rejected under 35 U.S.C 103(a) as being unpatentable over Betchtolsheim.

7. As per claims 5-7:

Betchtolsheim teaches the claimed limitations as mentioned above.

Betchtolsheim does not specifically teaches the CAM device wherein outputting the result signal in a first state comprises switchably coupling a match signal line to a predetermined voltage reference to affect a voltage level of the match signal line; outputting the result signal in the second state comprises decoupling the match signal line from the predetermined voltage reference; coupling a match signal line to a predetermined voltage reference comprises coupling the match signal line to a ground voltage reference to pull down the voltage level of the match signal line.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made because in the relational comparison logic circuit (equal to, less than and equal, greater than and equal, unequal), if the respective bit is greater or less than the stored bit, it means the match signal line is being applied by a predetermined level of voltage in order to activate the match signal line to produce a respective output signal [first state]. If the stored bit and respective bit are equal, it means the match signal line is being applied by a certain level of voltage (less than the predetermined level of voltage) in order to activate the match signal line to produce another respective output signal [second state]. In summary, in the event the data value is different from the comparand value, the node will be discharged (or charged) to a particular voltage. In the event the data value matches the comparand value, the node can remain charged (or discharged) to a ground voltage reference.

Claims 12 and 14 are rejected under 35 U.S.C 103(a) as being unpatentable over Betchtolsheim.

8. As per claim 12 and 14:

Betchtolsheim teaches the claimed limitations as mentioned above.

Betchtolsheim implicitly teaches the CAM device comprising a match line and wherein a most significant compare circuit of the plurality of compare circuits is coupled to the match line, the most significant compare circuit including circuitry to affect a logical state of the match line if either (1) a most significant bit of the first comparand value is greater than the most significant bit of the upper value, or (2) the most significant bit of the first comparand is equal to the most significant bit of the upper value, and a result signal from a less significant compare circuit of the plurality of compare circuits indicates that the first comparand value minus the value represented by the most significant bit of the first comparand value is greater than the upper value minus the value represented by the most significant bit of the upper value; the CAM device further comprising a match line and wherein a most significant compare circuit of the plurality of compare circuits is coupled to the match line, the most significant compare circuit including circuitry to affect a logical state of

the match line if either (1) a most significant bit of the first comparand value is less than the most significant bit of the lower value, or (2) the most significant bit of the first comparand is equal to the most significant bit of the lower value, and 'a result signal from a less significant compare circuit of the plurality of compare circuits indicates that the first comparand value minus the value represented by the most significant bit of the first comparand value is less than the lower value minus the value represented by the most significant bit of the lower value [col. 5, line 57 to col. 6, line 9]. This is This is because the whole limitations as mentioned above is only a relational comparison to see if the comparand after being compared is greater, less than the upper/lower bound, or equal the upper/lower bound.

Claims 16-17 and 19 are rejected under 35 U.S.C 103(a) as being unpatentable over Moughanni.

9. As per claims 16-17 and 19:

Moughanni teaches the claimed limitations as mentioned above.

Implicitly Moughanni teaches the Cam cells comprising an input to receive a second result signal from another CAM cell, and wherein the circuitry to output the first result signal in the first state is adapted to output the first result signal in the first state if the comparand value is equal to the first boundary value and the second result signal is in the first state; the circuitry to output the first result signal in the first state is further adapted to output the first result signal in the second state if the comparand value is equal to the first boundary value and the second result signal is in the second state; the CAM cells further comprising a third result signal from a less significant CAM cell, the circuitry to output the second result signal in the first state is further adapted to output the second result signal in the first state if the comparand value is equal to the second boundary value and the third result signal is in the first state [col. 4, lines 16-30; col. col. 4, line 61 to col. 5, line 35]. This is because the whole limitations as mentioned above is only a relational comparison to see if the comparand after being compared is greater than upper bound (as of claim 16), less than upper bound (as of claim 17), or the comparant is within the range (as of claim

19). In summary, if the comparant (hereinafter C) is equal to or greater than upper bound, then C is greater upper bound; if C is equal to and less than upper bound, then C is less than upper bound; if C is less than lower bound but greater than upper bound, and if C is greater than lower but less than upper bound, then C is within the range.

Claims 23-28, 35-39, 40-43 are rejected under 35 U.S.C 103(a) as being unpatentable over Betchtolsheim, and in view of Voelkel [PN 6,108,227].

10. As per claims 23-24, 35-39, 40-43:

Betchtolsheim teaches a system comprising a processor and a CAM [fig. 1]; a first and second storage circuits to store a first and second values a compare circuit for range comparison and for outputting a first result signal indicating whether the comparand value is greater than or equal to the first value; outputting the second result signal indicating whether the comparand is less than the second value; Betchtolsheim further teaches a CAM array having a plurality of CAM cells; the set of CAM cells being adapted to compare a comparand value to a range defined by at least one boundary value stored within the set of CAM cells, and the set of CAM cells being adapted to compare the comparand value for equality with a data value stored within the set of CAM cells.

Betchtolsheim does not specially teaches a mode select line coupled to at least one set of CAM cells; the mode select signal being either in the first or the second state; Voelkel teaches a mode select line [fig 1-2] coupled to at least one set of CAM cells; the mode select signal being either in the first or the second state [e.g., binary or ternary state]; the CAM device further comprising an interface to receive a first instruction from a host processor, the CAM device being adapted to store the first or second operating mode value in the storage circuit in response to the first instruction; the CAM cells is response to the mode select value to operate in either the first or second operating mode; the CAM device includes additional CAM cells configured to operate only in the second operating mode; the CAM device further comprising a mode select interface, and wherein the mode select line is coupled to the mode select

interface to receive the mode select signal from an external device host processor [abstract; col. 4, lines 35-65; col. 5, line 27 to col. 6, line 65; col. 7, line 39 to col. 8, line 60];

It would have been obvious to one having ordinary skill in the art at the time the invention was made to further include Voelkel 's teaching into Betchtolsheim's system. By combining range mode and ternary mode into a single CAM, wherein a mode select line embedded in the CAM for selecting which mode the CAM should be operated on, would allow a faster CAM comparison and less complex CAM structure design [col. 4, lines 14-25; col. 10, lines 50-55]. Combining different operating modes into a single CAM not only reduce cost and the complexity when designing CAM, but also increase the efficiency and flexibility of the CAM device. [col. 2, lines 1-10].

11. As per claims 25-28:

Betchtolsheim teaches the claimed limitations as mentioned above.

Betchtolsheim does not specially teach (if it is not implicitly teach) the CAM device further comprising circuit being adapted to selectively mask the first result signal, according to the second value, when the mode signal is in the second state; preventing the compare circuit from outputting the first result signal in a state indicative of inequality between the first value and the comparand; disabling the first value from being received in the compare circuit; disabling the comparand value from being received in the compare circuit.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made because when comparing data, if comparand bits do not match stored data bits (mismatch), the comparator should not generate the unnecessary mismatch signal, therefore the system does not waist additional processing cycles.

Claims 33-34, 46-47, 55-57 are rejected under 35 U.S.C 103(a) as being unpatentable over Moughanni, and in view of Voelkel.

12. As per claims 33-34, 46-47, 55-57:

Moughanni teaches the range operating mode [col. 4, lines 6-30] and the claimed limitations as mentioned above.

Moughanni dose not teach CAM cells are responsive to a mode select signal to operate in ternary mode or binary mode when the Cam cells being adapted to output the first result signal when operated in the range mode; the Cam device is responsive to the second instruction from the processor to store the mode value in the block configuration circuit.

Voelkel teaches CAM cells are responsive to a mode select signal to operate in either a ternary mode or binary mode; the CAM device is responsive to the second instruction from the processor to store the mode value in the block configuration circuit [col. 3, lines 30-65; col. 4, line 65 to col. 7, line 5].

It would have been obvious to one having ordinary skill in the art at the time the invention was made to further include Voelkel 's teaching into Moughanni's system. By combining range mode, binary mode and ternary mode into a single CAM, wherein a mode select line embedded in the CAM for selecting which mode the CAM should be operated on, would allow a faster CAM comparison and less complex CAM structure design [col. 4, lines 14-25; col. 10, lines 50-55]. Combining different operating modes into a single CAM not only reduce cost and the complexity when designing CAM, but also increase the efficiency and flexibility of the CAM device. [col. 2, lines 1-10].

Claim Objections

13. As per claim 44:

Claim 44 is objected to because of the following informalities: claim 44 is a duplicate of claim 43. Applicant is advised either to cancel claim 43 or 44 and renumber the claims accordingly.

14. As per claim 61:

The Examiner believes the limitation "the method of claim 61" is a typographical error. The Examiner assumes this limitation as -- the method of claim 58 --. Appropriate correction is required

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Miura et al PN 5,841,679 discloses CAM with upper/lower bit comparison.

b. Feldmeier et al PN 6,289,414 discloses Ternary CAM for searching.

c. Sherman PN 6,389,507 discloses CAM with range searching.

d. Hallberstam et al PN 5,561,429 discloses CAM with range searching including lower registers for lower bound and upper registers for upper bound.

e. Gray PN 6,483,732 discloses Relational CAM.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ngoc Dinh whose telephone number is (703) 305-3023. The examiner can normally be reached on Monday-Friday 8:30 AM-5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks, can be reached on (703) 308-1756. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

NGOC DINH
Patent examiner
Art Unit 2187
September 04, 2003

DONALD A. SPARKS
Supervisor Patent Examiner
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